# Measurements of Breakdown Field and Forward Current Stability in 3C-SiC pn Junction Diodes Grown on Step-Free 4H-SiC

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**Abstract.** This paper reports on initial fabrication and electrical characterization of 3C-SiC $p^+n$ junction diodes grown on step-free 4H-SiC mesas. Diodes with n-blocking-layer doping ranging from ~ $2 \times 10^{16}$ cm$^{-3}$ to ~ $5 \times 10^{17}$ cm$^{-3}$ were fabricated and tested. No optimization of junction edge termination or ohmic contacts was employed. Room temperature reverse characteristics of the best devices show excellent low-leakage behavior, below previous 3C-SiC devices produced by other growth techniques, until the onset of a sharp breakdown knee. The resulting estimated breakdown field of 3C-SiC is at least twice the breakdown field of silicon, but is only around half the breakdown field of <0001> 4H-SiC for the doping range studied. Initial high current stressing of 3C diodes at 100 A/cm$^2$ for more than 20 hours resulted in less than 50 mV change in ~ 3 V forward voltage.

## Introduction

Recent advancements in cubic-SiC crystal growth and MOSFET properties have renewed interest in the 3C polytype for realizing beneficial high power and/or high temperature electronics [1-3]. Until recently, 3C-SiC extended defect densities were too high to support fabrication of even small-area 3C-SiC devices free of dislocations. Step-free surface heteroepitaxy has enabled dislocation-free layers of 3C-SiC to be realized on top of small device-sized mesas arrayed across on-axis 4H-SiC wafers [3]. This paper reports on fabrication and electrical characterization of breakdown field and forward bias current stability of an initial lot of small-area epitaxial 3C-SiC $p^+n$ junction diodes grown on step-free 4H-SiC mesas.

## Experimental

Fig. 1 shows a simplified schematic cross-section of the $p^+n$ junction diodes that were studied. The buried 3C/4H heterojunction was grown with heavy n-type doping in order to minimize its impact on top contact to backside contact (Fig. 1b) electrical measurements. The diodes were fabricated starting from a quarter of a commercially purchased on-axis 4H-SiC wafer [4]. Except as noted below, the epitaxial growth processes employed, namely step free surface heteroepitaxy [3] and site-competition doping [5], have been previously described. Patterned etching of trenches to a depth of ~10 μm to form pre-growth mesas arrayed across the wafer was carried out by the wafer vendor [4]. The wafer was piranha cleaned and loaded into a modified horizontal-flow single-wafer cold-wall chemical vapor deposition system with an inductively heated stationary (no rotation) uncoated graphite susceptor [6]. An in-situ pre-growth etch was performed at ~1200 °C with 120 sccm HCl diluted in 4 slm of H$_2$ [3,7]. The substrate temperature was then ramped over 5 minutes to ~1500 °C and step-flow growth carried out by flowing 6.7 sccm N$_2$, 2.7 sccm SiH$_4$ and 3 sccm C$_3$H$_8$ (Si/C ratio of 0.9). For mesas not threaded by substrate screw dislocations, this step produces
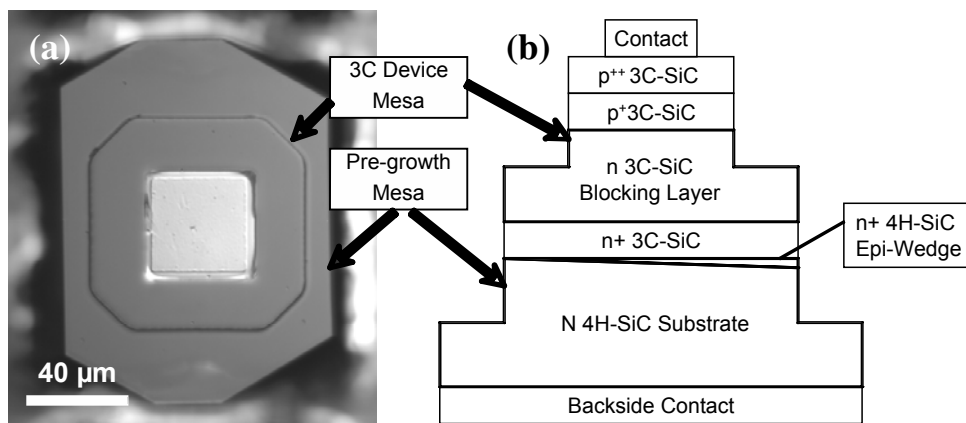
**Fig. 1.** (a) Optical microscope photo top view and (b) simplified schematic cross-sectional depiction of 3C-SiC p$^+$n junction diode structure grown on top of step-free 4H-SiC mesa studied in this work. For simplicity, SiC deposition on pre-growth mesa sidewalls is not shown in (b).

a heavily doped n$^+$ 4H-SiC epi-wedge with atomically flat top surface (Fig. 1) [3]. The substrate temperature was then lowered to ~1380 °C over 10 minutes to ensure nucleation of high quality 3C-SiC heteroepilayer [3], and then increased to ~1410 °C over 2 minutes where it remained for the rest of the 3C-SiC layer growth. The n$^+$ 3C-SiC layer was grown for 15 minutes at these conditions, followed by 3 hours of lighter-doped n 3C-SiC blocking layer growth under reduced N$_2$ flow of 0.25 sccm. The p$^+$ layer was then grown by eliminating the N$_2$, reducing the SiH$_4$ to 1.5 sccm (Si/C ratio of 0.5), and adding 0.5 sccm trimethylaluminum (TMAl) for 15 minutes [5]. Process test films grown in these conditions yielded ~$10^{18}$ cm$^{-3}$ p-type and growth rates near 1.2 μm/hour. An even heavier-doped p$^{++}$ 3C-SiC layer (> $10^{19}$ cm$^{-3}$) to assist p-type ohmic contact formation was then grown for 30 minutes by increasing the TMAl to 4 sccm's. In the final minute of growth, the SiH$_4$ flow was cutoff to promote surface Al dopant saturation [5].

Following growth the quarter-wafer piece was surveyed by differential interference contrast (DIC) optical microscopy to verify formation of at least a few mesas with lateral cantilevers and smooth double-positioning boundary (DPB) free surface morphology expected for high-quality 3C-SiC mesa heterofilms [3]. Unfortunately, the particular 4H-SiC commercial substrate used for this initial experiment suffered from unusually high axial screw dislocation density (well over 2 x $10^4$ cm$^{-2}$), so that only a little more than a dozen out of ~ 300 of the smallest pre-growth mesas with diodes on them yielded the expected good 3C-SiC film morphology.

In order to fully isolate the 3C p$^+$n junction, a Ti/Ni metal etch mask was patterned and the mesa epilayers were reactive ion etched to a depth of ~ 3 μm in a fluorine plasma. The etch mask was then stripped and the sample piranha cleaned prior to depositing Ti/TaSi$_2$/Pt as a backside metal contact [8]. Prior to topside ohmic contact deposition, the quarter wafer was sawed in half and one piece was set aside. Thin Al/Ti/Al (5nm/10nm/10nm) layers were electron beam deposited at 7 x $10^{-8}$ Torr, patterned via wet etching, and annealed in a tube furnace at 800 °C for 30 minutes in an Ar atmosphere. Ti/Ni (25nm/200nm) was then deposited and patterned by lift-off on top of the thin annealed Al/Ti/Al to finish the p-type top diode contact. No optimization of junction edge termination or ohmic contacts was employed.

Electrical results summarized in this paper were recorded from six high-quality small-area (A = 5.9 x $10^{-5}$ cm$^2$) 3C diodes that were not threaded by the high density of underlying 4H-SiC substrate screw dislocations. Electrical characterization was carried out in near-dark conditions at room temperature on a probing station using computer-controlled source-measure units and 1 MHz capacitance bridge.

## Results and Discussion

Consistent with previous work [9], the 3C-SiC p$^+$n junction diodes emitted yellow-green light observable with the naked eye under sufficient (> 2 mA) forward bias. C-V measurements revealed

that the doping of the lighter-doped n-side of the junction systematically varied from ~2 x $10^{16}$ cm$^{-3}$ on one side of the wafer to ~5 x $10^{17}$ cm$^{-3}$ on the other, which was not unexpected for the growth reactor configuration that used un-coated graphite susceptor and no sample rotation.

The reverse I-V behavior of devices spanning the measured blocking-layer doping



**Fig. 2.** Measured reverse I-V characteristics at 25 °C on six 3C-SiC p$^+$n junction diodes with various n-layer dopings.



**Fig. 3.** Breakdown electric field as a function of n-layer doping (see text).

range is shown in Fig. 2. Excellent reverse-leakage behavior, below the measurement noise floor for the majority of the sweeps, was observed. It is worth noting that leakage current densities shown in Fig. 2 are significantly less than the previous lowest leakage for 3C-SiC p$^+$n diodes of similar blocking voltage [9]. The reverse I-V curves of Fig. 2 also exhibit a sharp breakdown knee characterized by more than 50X current increase per volt at breakdown. The breakdown voltage did not degrade with multiple measurement sweeps with instrument current compliance limit set to 2 A/cm$^2$. As expected, the 3C-SiC p$^+$n junction diode breakdown voltage increased as measured blocking layer doping decreased.

The peak electric field E$_B$ in each diode at breakdown can be estimated using the well-known procedure described in [10] with doping N$_A$ extracted from C-V measurements and I-V measured breakdown voltage knee V$_B$ apparent from Fig. 2. The hollow plus symbols plotted in Fig. 3 show the resulting breakdown field calculated for the six 3C-SiC devices as a function of measured blocking n-layer doping. For comparison, Fig. 3 also plots previously reported diode breakdown fields from 4H-SiC [11,12], other previously reported 3C-SiC samples [9,13], and silicon [10]. The Fig. 3 experimental results indicate that the breakdown field of n-type 3C-SiC is at least twice the breakdown field of silicon, but is only around half the breakdown field of <0001> 4H-SiC for the doping range studied.

Fig. 4 shows the forward bias behavior of two devices both before (solid lines) and after (dashed lines) prolonged (> 20 hour) forward-bias stressing at 100 A/cm$^2$. For currents above ~ 1 A/cm$^2$, the forward I-V characteristics before and after stressing are virtually identical. Interestingly, the stressing removed a low-current conduction hump evident in the 4.7 x $10^{17}$ cm$^{-3}$ pre-stress I-V. The saturation current density J$_0$ and diode ideality factor n > 2 (Fig. 4) are higher than might be expected for nominal 3C-SiC pn junction diodes. Because it is effectively in series with the 3C p$^+$n junction, it seems unlikely that the buried 3C/4H heterojunction would cause diode current (i.e., J$_0$) to increase. Lacking larger device
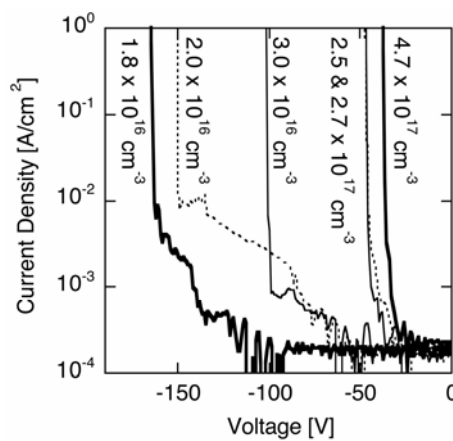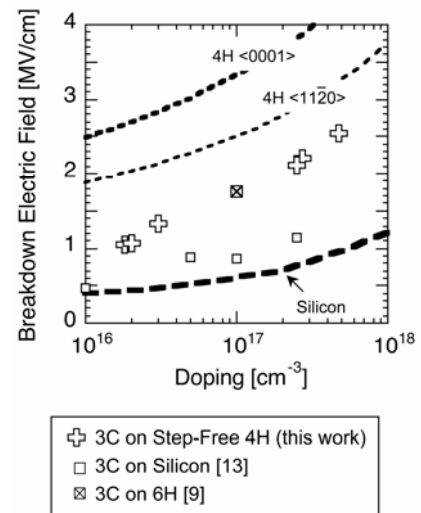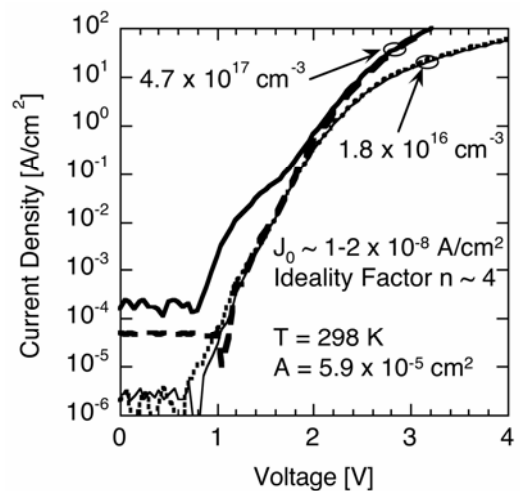


**Fig. 4.** Forward current vs. voltage plots of two 3C-SiC p$^+$n diodes before (solid lines) and after (dashed lines) bias stressing at 100 A/cm$^2$.

sizes to test perimeter-to-area leakage effects, we are left at this time to conjecture that perhaps some forward I-V non-idealities may arise from surface current effects around the etched diode periphery in these small-area (i.e., large perimeter-to-area ratio) devices.

Fig. 5 summarizes forward current bias stress tests conducted on four of the 3C $p^+n$ diodes. In particular, Fig. 5 plots the applied forward voltage $V_F$ required to maintain 100 A/cm$^2$ current as a function of time. All devices tested were highly stable in that $V_F$ changed less than 50 mV for all tests. Thus, these small-area 3C devices do not exhibit high forward current instability observed in 4H-SiC bipolar junction diodes [14]. However, no conclusions on relative stability of 3C-SiC versus 4H-SiC against bipolar recombination enhanced degradation should yet be drawn from this very limited initial study of very small area 3C diodes with relatively low blocking voltage compared to degradation observed in large-area high blocking voltage 4H-SiC diodes.
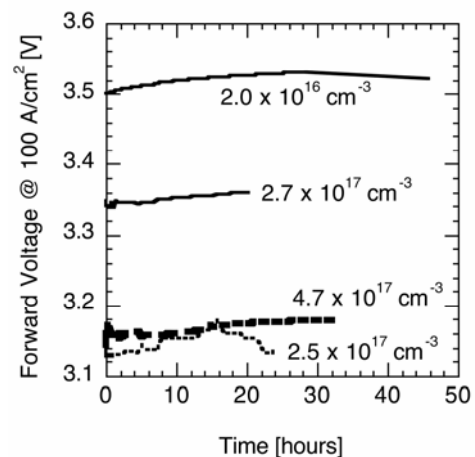


**Fig. 5.** Forward voltage required to maintain 100 A/cm$^2$ current flow versus stress time for four 3C-SiC $p^+n$ diodes with various blocking layer dopings.

## Summary

The electrical performance of 3C-SiC bipolar $p^+n$ junction diodes fabricated from high quality mesa heterofilms has been studied. For the 3C-SiC polytype, the diodes exhibit state of the art low reverse leakage, high breakdown electric field, and stable forward voltage at high current density.

## References
[1]   J. Wan, et al.: IEEE Electron Device Lett. Vol. 23 (2002), p. 482.
[2]   H. Nagasawa, et al.: in *Silicon Carbide: Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, Eds. (Springer-Verlag, Berlin 2003), p. 207.
[3]   P. G. Neudeck and J. A. Powell: in *Silicon Carbide: Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, Eds. (Springer-Verlag, Berlin 2003), p. 179.
[4]   Cree, Inc.: Durham, NC USA, http://www.cree.com.
[5]   D. J. Larkin: Phys. Stat. Sol. A Vol. 202 (1997), p. 305.
[6]   Aixtron Inc.: Model AIX 200/4 HT, http://www.aixtron.com.
[7]   J. A. Powell, et al.: Appl. Phys. Lett. Vol. 59 (1991), p. 333.
[8]   R. S. Okojie, et al.: J. Appl. Phys. Vol. 91 (2002), p. 6553.
[9]   P. G. Neudeck, et al.: IEEE Trans. Electron Devices Vol. 41 (1994), p. 826.
[10]  B. J. Baliga, Modern Power Devices, 1st ed. (Wiley & Sons: New York, 1987), p. 67.
[11]  A. O. Konstantinov, et. al.: Appl. Phys. Lett. Vol. 71 (1997), p. 90.
[12]  S. Nakamura, et. al.: J. Appl. Phys. Vol. 80 (2002), p. 3355.
[13]  C. W. Liu and J. C. Sturm: J. Appl. Phys. Vol. 82 (1997), p. 4558.
[14]  S. Ha and J. P. Bergman: MRS Bulletin Vol. 30 (2005), p. 305.